

wherein said data transfer switch further comprises a plurality of buses.

REMARKS

Claims 19-44 are pending.

Claims 19-44 stand rejected.

Claims 19 and 28 have been amended.

No new matter has been added.

Claims 19-44 are hereby submitted for reconsideration.

In paragraph 3 of the Office Action, the Examiner has rejected claims 41 and 42 under 35 U.S.C. § 112 for failing to comply with the written description requirement. Applicants disagree with the Examiner's contention and note that the element of "a plurality of modules including an interface unit, which is capable of controlling a first host processor" is supported in the specification as filed.

Applicants note that page 15 of the specification, lines 15-20 state:

"Multimedia processor 100 can function as either a master or a slave device when coupled to either PCI or AGP (accelerated Graphics Port) bus via interface unit 130. Because the two buses can be coupled to multimedia processor 100 independent from each other, multimedia processor 100 can operate as the bus master device on one channel and a slave device on the other. To this end multimedia processor 100 appears as a multifunction PCI/AGP device, when it operates as a slave device from the point of a host system."

The host system of the PC (corresponding to the first processor) could generally be either a master of the PCI bus or a slave thereof. For these reasons, the multimedia processor 100 and the PCI/AGP interface 130 fall under the plurality of processors

capable of controlling the host processor.

As such, Applicants respectfully request that the rejection of claims 41 and 42 be withdrawn.

In paragraph 6 of the Office Action, the Examiner has rejected claims 19-44 under 35 U.S.C. § 103 as being unpatentable over Gibson (U.S. Patent No. 6,414,687) in view of Kusters (U.S. Patent No. 5,819,112).

In forming the rejection, the Examiner has asserted that the components of Gibson correspond to the components of the present invention except for the multiplexer where he turns to Kusters, claiming that it would be obvious to combine the multiplexer of Kusters with the processor from Gibson to arrive at the present invention as claimed.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

The present invention as claimed is directed to an integrated multimedia system. Among other components, the multimedia system of the present invention includes a data transfer switch disposed within the multimedia processor, coupled to the second processor for transferring data to various modules of the processor, where the data transfer switch is configured to transfer data between the modules of the multimedia processor *in either direction between at least two modules within the multimedia processor as requested by said modules.*

Such an arrangement is described on pages 18 and 19 of the specification and in particular on lines 1-2 of page 19. A more elaborate description of the function of the data transfer switch is found on 29-32 and in accompanying Figs. 2, 3A and 3B of the present invention.

This configuration for the data transfer switch allows for data transfers to occur between components within the multimedia processor in different non-predefined directions. Thus, a data transfer between a first and second component may occur in one direction and a subsequent data transfer may occur through the same data transfer switch between the same two components in the opposite direction.

The cited prior art, namely Gibson teaches an integrated multimedia system having a raster image coprocessor 223 disposed on an integrated ASIC chip 220, a host CPU 202 as shown in Fig. 1. The raster image co-processor maintains a results organizer 249 and an input interface switch 252 which the Examiner has equated to the data transfer switch of the present invention.

In Gibson, the results organizer 249 receives a result from the JPEG coder/decoder 241 and the main data path 242, and transmits the result to one of the external interface controllers 238, the local memory controller 236 and the peripheral interface controller 237. The input interface switch 252 receives data from the controllers 236 and 238 and outputs to the controllers 235 and 240. The result of such a structure is that organizer 249 and input interface switch 252 perform data transfer from one of several input side devices in a *in a single predefined direction* to one of a plurality of output side devices. See column 9, line 45 to column 10, line 4 of Gibson.

Applicants note that Kusters was cited to by the Examiner to support the portion of the argument related to the multiplexer, and does not contain a data transfer switch similar to that in the present invention.

As such, the cited prior art, either alone or in combination with one another, teach or suggest the present invention as claimed, because neither reference contains a teaching

for a data transfer switch for transferring data to various modules, where the data transfer switch transfers data between the modules of the multimedia processor in either direction between at least two modules within said multimedia processor as requested by said modules.

For at least this reason, Applicants respectfully request that the rejection of independent claims 19 and 28 and the claims that depend therefrom be withdrawn.

In addition to the above outlined argument, Applicants further note that the Examiner indicated the Gibson did not show a multiplexer as per the claimed invention, but instead relies on Kuster for this portion of the rejection.

However, the present invention teaches a multiplexer coupled to the interface unit for providing access between a selected number of the I/O device driver units to external I/O devices via output pins. See Fig. 1B of the present invention. Thus, the present invention ***allows access*** between the plurality of I/O devices and the selected number of I/O devices. See pages 24-26 of the specification.

Rather, Kusters teaches a multiplexer 30 that is simply for validating an access between a non-predefined type of I/O device, such as a display device and the device driver thereof. See column 15, line 62 to column 16, line 13 of Kusters for a description of the validation process. Here the multiplexer is allowing the class device drivers, such as 38x, supports its peripheral I/O devices 32, upon a queue arrangement. This is not analogous to the multiplexer of the present invention.

As such, neither the cited prior art, either alone or in combination with one another, teach or suggest the present invention as claimed, because neither reference contains a teaching for a multiplexer coupled to the interface unit for providing access

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between a selected number of the I/O device driver units to external I/O devices via output pins.

For at least this reason, Applicants respectfully request that the rejection of independent claims 19 and 28 and the claims that depend therefrom be withdrawn.

In paragraph 9 of the Office Action, the Examiner has rejected claims 19-44 under the judicially created doctrine of obviousness type double patent in view of the co-pending application Serial No. 10/867,868 in view of Gibson. Applicants have filed an appropriate terminal disclaimer herewith and respectfully request that this rejection be withdrawn.

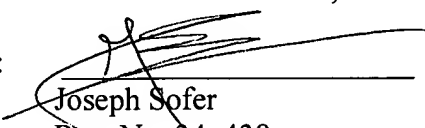
In view of the forgoing, Applicants respectfully submit that the present invention as claimed is now in condition for allowance, the earliest possible notice of which is earnestly solicited. If the Examiner feels that a telephone interview would advance the prosecution of this application he is invited to contact the undersigned at the number listed below.

Respectfully submitted

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